CLAIMS

What is claimed is:

1. A method of forming a semiconductor device, comprising:

providing a structure having a first critical dimension;

forming a lithographic pattern on said structure; and

etching said structure with an O_2-containing material to trim said first critical dimension to a second critical dimension, said second critical dimension being smaller than said first critical dimension.

2. The method of claim 1, further comprising:

correcting an offset between a nested feature printed on said structure and an isolated feature printed on said structure

3. The method of claim 1, further comprising:

forming a positive photoresist over said structure prior to forming said lithographic pattern on said structure.

4. The method of claim 2, wherein said correcting includes:

forming a negative photoresist over said nested feature and said isolated feature; and

etching said semiconductor substrate using a surface charging technique in combination with a plasma etch, such that said nested feature is etched faster than said isolated feature.

5. The method of claim 1, wherein said second critical dimension is within a range of about 10-50 nm smaller than said first critical dimension.

6. The method of claim 1, wherein said etching is performed at approximately 5mT to approximately 50mT for a time of between approximately 5 seconds to approximately 40 seconds.

7. The method of claim 1, wherein said structure includes an anti-reflection coating formed on a polysilicon substrate.

8. A method of trimming a conductor on a substrate, comprising:

providing a conductor having a first critical dimension;

forming a lithographic pattern on said conductor; and

etching said conductor with an O_2-containing material to trim said first critical dimension to a second critical dimension, said second critical dimension being smaller than said first critical dimension.

9. The method of claim 8, further comprising:

correcting an offset between a nested feature printed on said conductor and an isolated feature printed on said conductor.

10. The method of claim 8, further comprising:

forming a positive photoresist over said conductor prior to forming said lithographic pattern on said conductor.

11. The method of claim 8, wherein said second critical dimension is within a range of about 10-50 nm smaller than said first critical dimension.

12. The method of claim 8, wherein said etching is performed at approximately 5mT to approximately 50mT for a time of between approximately 5 seconds to approximately 40 seconds.

13. The method of claim 8, wherein said conductor includes a polysilicon substrate having an anti-reflection coating formed thereon.

14. A method of etching a semiconductor device, comprising:

etching said semiconductor device using a surface charging technique in combination with a plasma etch, such that a nested feature formed on said

semiconductor device is etched faster than an isolated feature formed on said semiconductor device.

15. The method of claim 14, wherein said etching said nested feature faster corrects an offset between said nested feature and said isolated feature.

16. The method of claim 14, wherein a negative photoresist is provided over said nested feature and said isolated feature.

17. The method of claim 14, wherein said etching uses a mixture of NF_3 and argon.

18. The method of claim 14, wherein said semiconductor device includes a polysilicon substrate, a TEOS layer formed over the substrate, and an antireflection coating layer formed over the substrate.

19. A method of etching a semiconductor material, comprising:

providing a semiconductor substrate including a nested feature and an isolated feature;

forming a negative photoresist over said nested feature and said isolated feature; and

etching said semiconductor substrate using a surface charging technique in combination with a plasma etch, such that said nested feature is etched faster than said isolated feature.

20. The method of claim 19, wherein said semiconductor substrate includes a polysilicon substrate, and wherein a TEOS layer and an antireflection coating layer are formed over the substrate.